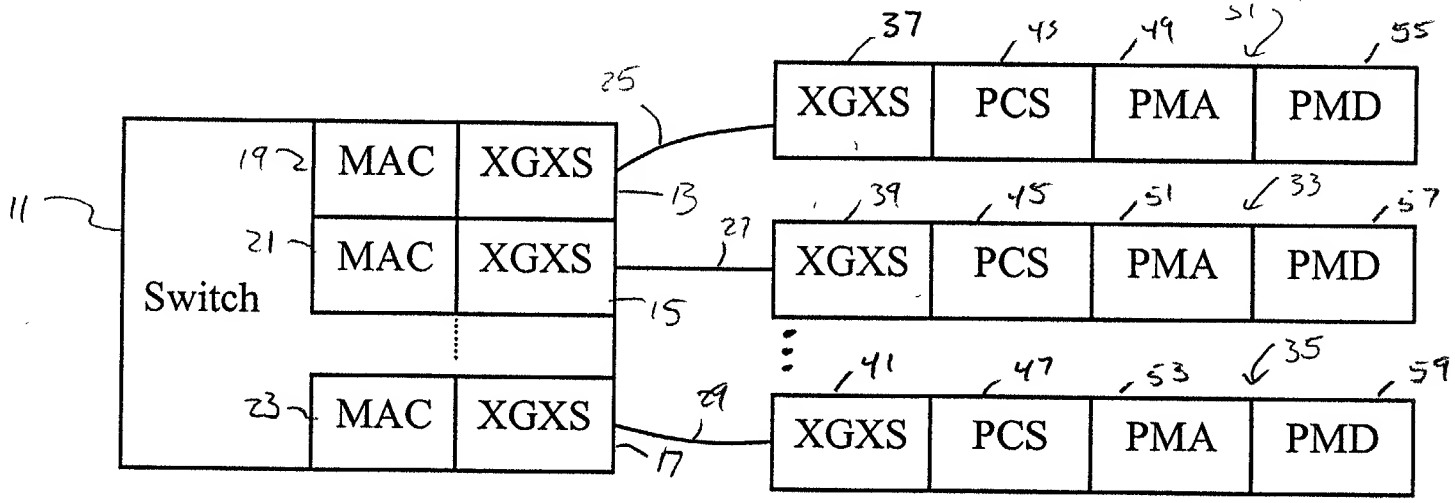

Figure 1.

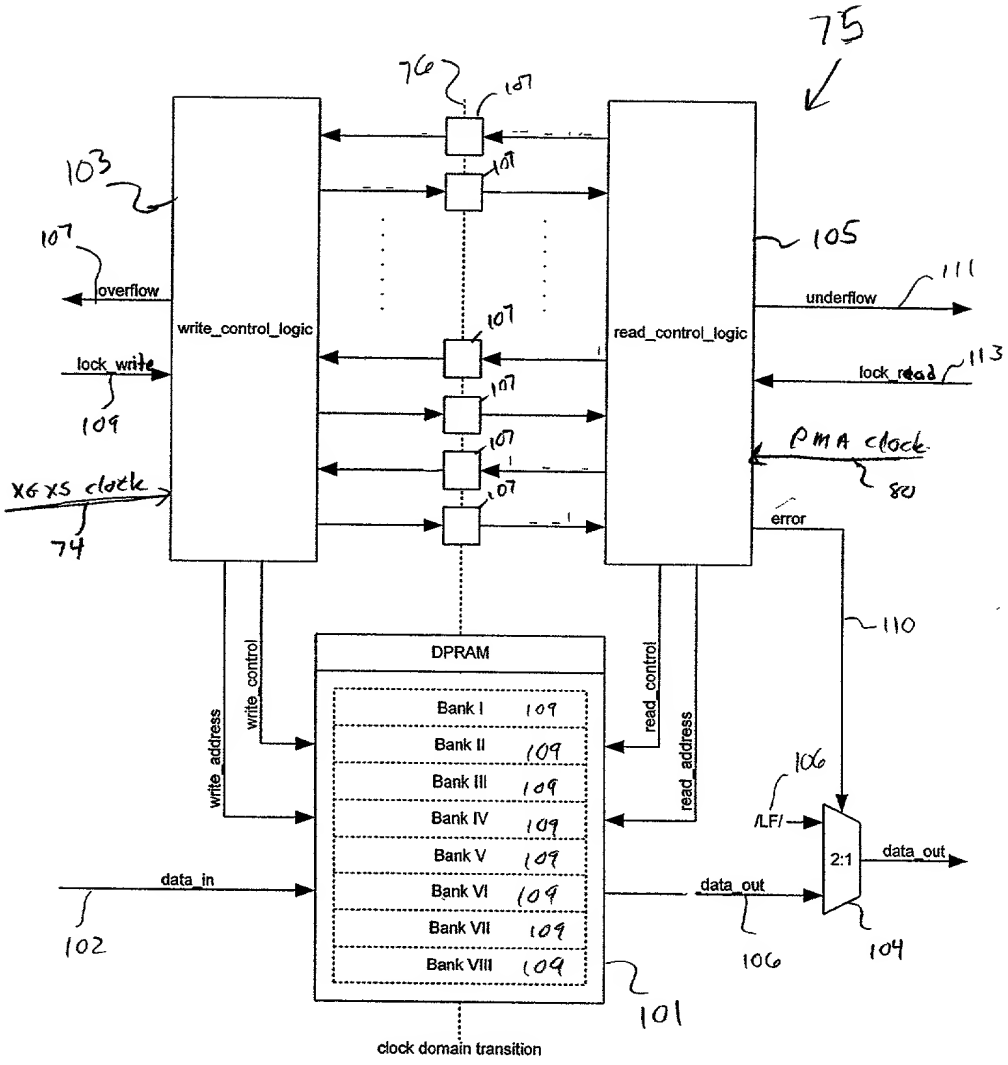
75
76
107
103
105
overflow
write_control_logic
read_control_logic
underflow
111
lock_write
109
lock_read
113
PMA clock
80
X6 XS clock
74
error
110
DPRAM
write_control
write_address
read_control
read_address
Bank I 109
Bank II 109
Bank III 109
Bank IV 109
Bank V 109
Bank VI 109
Bank VII 109
Bank VIII 109
106
/LF/
2:1
data_out
data_in
102
data_out
106
104
101
clock domain transition

Figure 3

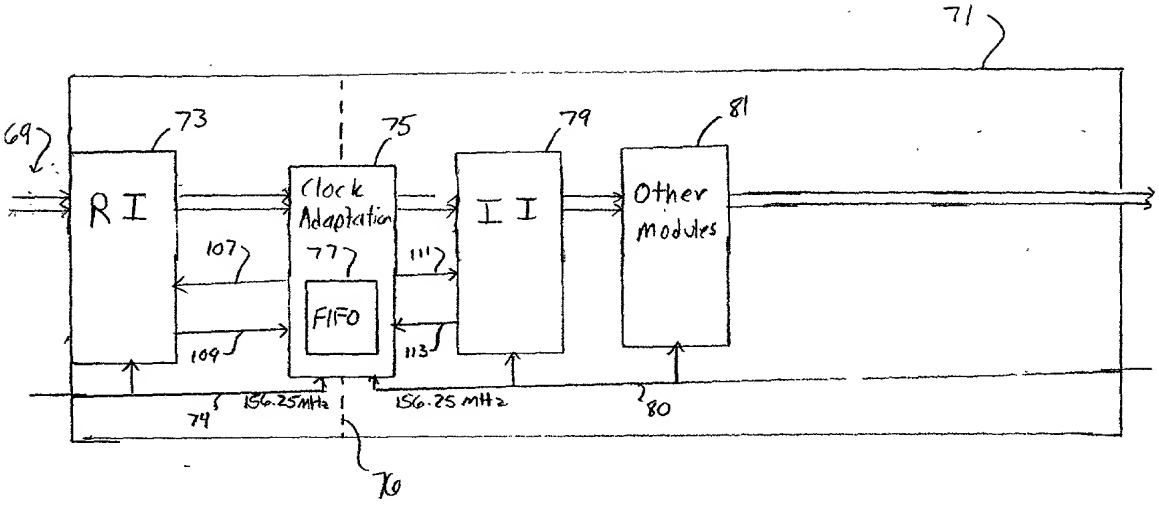
71
69
73
RI
75
Clock Adaptation
77
FIFO
79
II
81
Other modules
107
109
111
113
74
156.25 MHz
156.25 MHz
80
76

Fig. 2

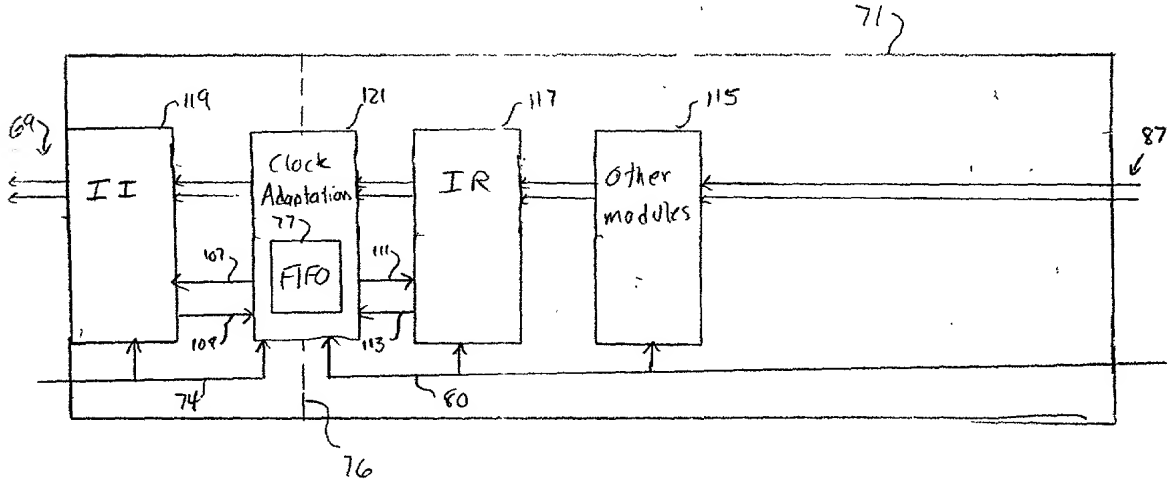
71
69
119
II
121
Clock Adaptation
77
FIFO
117
IR
115
Other modules
87
107
109
111
113
74
80
76

Fig. 4